Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A calibration circuit for adjusting a common electrode voltage Vcom for a liquid crystal display (LCD), comprising a controller to receive a first command for changing said common electrode voltage Vcom by way of a single-wire interface, and to cause said common electrode voltage Vcom to change in response to said first command, the controller having a counter to generate a count related to said common electrode voltage Vcom, and a digital-to-analog converter (DAC) to generate an intermediate voltage related to said count.

Claims 2-4 (Canceled)

5. (Currently Amended) The calibration circuit of claim [[4]]1, further comprising a current-steering circuit to steer a current related to said common electrode voltage Vcom in response to said intermediate voltage.

6. (Original) The calibration circuit of claim 5, wherein said current-steering circuit comprises:

a field effect transistor (FET) including a drain, a gate, and a source;

an operational amplifier including a first input to receive said intermediate voltage, a second input coupled to the source of said FET, and an output coupled to the gate of said FET.

7. (Original) The calibration circuit of claim 6, further comprising a current-setting resistor coupled to the source of said FET.

8. (Original) The calibration circuit of claim 7, further comprising a voltage divider including an intermediate node coupled to a drain of said FET.

9. (Original) The calibration circuit of claim 8, further comprising a buffer coupled to said intermediate node of said voltage divider.

10. (Currently Amended) The calibration circuit of claim [[2]]1, further comprising a non-volatile memory for storing said count.

11. (Original) The calibration circuit of claim 10, wherein said non-volatile memory comprises an electrically erasable programmable read only memory (EEPROM).

12. (Original) The calibration circuit of claim 10, wherein said controller causes said count of said counter to be rewritten into said non-volatile memory in response to a second command received by way of said single-wire interface.

13. (Original) The calibration circuit of claim 12, wherein said second command comprises a voltage greater than a predetermined threshold.

14. (Original) The calibration circuit of claim 13, further comprising a comparator to compare said second command voltage to said threshold, and to generate a signal for said controller if said second command voltage is greater than said threshold.

15. (Original) The calibration circuit of claim 13, wherein said non-volatile memory is configured to receive said second command voltage for use in storing said count into said non-volatile.

16. (Original) The calibration circuit of claim 1, wherein said controller includes an enable input for receiving a second command which causes said controller to ignore said first command.

17. (Original) The calibration circuit of claim 1, further comprising a low power mode circuit to reduce a power consumption of said calibration circuit.

18. (Currently Amended) A method of adjusting a common electrode voltage Vcom of a liquid crystal display (LCD), comprising:

generating a count related to said common electrode voltage Vcom;

receiving a first command to change said count in a first direction to increase said common electrode voltage Vcom by way of a single-wire interface;

increasing said common electrode voltage Vcom in response to said count ~~first command;~~

receiving a second command to change said count in a second direction to decrease said common electrode voltage Vcom by way of said single-wire interface; and

decreasing said common electrode voltage Vcom in response to said count; ~~second command~~

receiving a third command to store said count in a non-volatile memory by way of said single-wire interface;

storing said count in said non-volatile memory in response to said third command.

Claims 19-21 (Canceled)

22. (Currently Amended) The method of claim ~~19~~18, further comprising decrementing said count in response to said first command.

23. (Currently Amended) The method of claim ~~19~~18, further comprising incrementing said count in response to said second command.

24. (Original) The method of claim 18, wherein said first command comprises a pulse.

25. (Original) The method of claim 24, wherein a maximum amplitude of said pulse is above a predetermined amplitude threshold to indicate that said first command is for increasing the common electrode voltage Vcom.

26. (Original) The method of claim 24, wherein a width of said pulse is above a predetermined width threshold to indicate that said pulse is not to be ignored.

27. (Currently Amended) The method of claim ~~19~~18, wherein said second command comprises a pulse.

28. (Original) The method of claim 27, wherein a minimum amplitude of said pulse is below a predetermined amplitude threshold to indicate that said second command is for decreasing the common electrode voltage Vcom.

29. (Original) The method of claim 28, wherein a width of said pulse is above a predetermined width threshold to indicate that said pulse is not to be ignored.

30. (Currently Amended) The method of claim ~~20~~18, wherein said third command comprises a voltage above a predetermined voltage threshold.

31. (Original) The method of claim 30, further comprising using said voltage to program a storing of said count into said non-volatile memory.

32. (Currently Amended) The method of claim ~~19~~18, further comprising:

receiving a pulse by way of said single-wire interface; and

ignoring said pulse if a width of said pulse is below a predetermined width threshold.

33. (Currently Amended) The method of claim ~~19~~18, further comprising:

receiving a ~~third~~ fourth command to disable a processing of said first and second commands;

receiving a ~~fourth~~ fifth command to increase or decrease said common electrode voltage Vcom by way of said single-wire interface; and

ignoring said ~~fourth~~ fifth command in response to said ~~third~~ fourth command.

Claims 34-36 (Canceled)

37. (Previously Presented) A calibration circuit for use in adjusting a common electrode voltage Vcom for a liquid crystal display (LCD) comprising:

a controller to receive commands by way of a single-wire interface;

an up/down counter coupled to the controller;

electrically reprogrammable nonvolatile storage coupled to the controller and to an output of the up/down counter;

a digital to analog converter (DAC) having an input coupled to the output of the up/down counter, an output of the DAC being coupled to provide a calibration circuit output;

the up/down counter having a power on reset for resetting the counter to a count stored in the nonvolatile storage on application of power to the calibration circuit;

the controller being responsive to a first command from the single wire interface to cause the counter to increase its count;

the controller being responsive to a second command from the single wire interface to cause the counter to decrease its count;

the controller being responsive to a third command from the single wire interface to cause the nonvolatile storage to store a count from the up/down counter.

38. (Previously Presented) The calibration circuit of claim 37 wherein the first and second commands are voltage pulses in first and second directions, respectively, of at least a predetermined duration.

39. (Previously Presented) The calibration circuit of claim 38 wherein the first command is sensed by sensing a voltage from the single wire interface relative to a threshold voltage.

40. (Previously Presented) The calibration circuit of claim 38 wherein the second command is sensed by sensing a voltage from the single wire interface relative to a threshold voltage.

41. (Previously Presented) The calibration circuit of claim 38 wherein the first and second commands are each voltage pulses of decreased and increased voltages, respectively.

42. (Previously Presented) The calibration circuit of claim 41 wherein the third command comprises a programming voltage pulse for the nonvolatile storage.

43. (Previously Presented) The calibration circuit of claim 42 wherein the third command is a positive going programming voltage pulse of greater amplitude than the second command, the controller being configured to distinguish between the second and third commands by sensing a positive pulse rising to a voltage above a second command voltage in less than the predetermined duration.

44. (Previously Presented) The calibration circuit of claim 43 wherein the predetermined duration is 200 μsec.

45. (Previously Presented) The calibration circuit of claim 38 wherein the third command comprises a programming voltage pulse for the nonvolatile storage.

46. (Previously Presented) The calibration circuit of claim 45 wherein the electrically reprogrammable nonvolatile storage is an EEPROM.

47. (Previously Presented) The calibration circuit of claim 38 wherein the first and second commands are each voltage pulses of decreased and increased voltages, respectively, relative to a threshold voltage.

48. (Previously Presented) The calibration circuit of claim 37 wherein the calibration circuit output is configured to provide an adjustable output current sink.

49. (Previously Presented) The calibration circuit of claim 48 wherein the adjustable output current sink is configured to sink more current responsive to an increase in the count in the up/down counter.

50. (Previously Presented) The calibration circuit of claim 37 wherein the controller is responsive to the first, second and third commands only when a controller enable signal received on a controller enable terminal enables the controller.

51. (Previously Presented) The calibration circuit of claim 37 wherein the calibration circuit is a single integrated circuit.

52. (Previously Presented) A calibration circuit for use in adjusting a common electrode voltage Vcom for a liquid crystal display (LCD) comprising:

a controller coupled to receive commands by way of a single-wire interface;

an up/down counter coupled to the controller;

electrically reprogrammable nonvolatile storage coupled to the controller and to an output of the up/down counter;

a digital to analog converter (DAC) having an input coupled to the output of the up/down counter, an output of the DAC being coupled to provide an adjustable calibration circuit current sink output;

the up/down counter having a power on reset for resetting the counter to a count stored in the nonvolatile storage on application of power to the calibration circuit;

the controller being responsive to a first pulse of reduced voltage from the single wire interface relative to a threshold voltage for at least a predetermined time to cause the counter to increase its count;

the controller being responsive to a second pulse of increased voltage from the single wire interface relative to a threshold voltage for at least a predetermined time to cause the counter to decrease its count;

the controller being responsive to a programming voltage pulse from the single wire interface to cause the nonvolatile storage to store a count from the up/down counter, the controller being configured to distinguish between the programming voltage pulse and the second pulse by sensing the rise in voltage above a voltage exceeding the voltage of a first pulse in less than the predetermined time.

53. (Previously Presented) The calibration circuit of claim 52 wherein the predetermined duration is 200 μsec.

54. (Previously Presented) The calibration circuit of claim 52 wherein the electrically reprogrammable nonvolatile storage is an EEPROM.

55. (Previously Presented) The calibration circuit of claim 52 wherein the adjustable output current sink is configured to sink more current responsive to an increase in the count in the up/down counter.

56. (Previously Presented) The calibration circuit of claim 52 wherein the controller will be responsive to the first, second and third commands only when a controller enable signal received on a controller enable terminal enables the controller.

57. (Previously Presented) The calibration circuit of claim 52 wherein the calibration circuit is a single integrated circuit.